

CLAIMS

What is claimed is:

- 1 1. A method for producing a die assembly comprising the steps of:
2 providing a wafer stack defining a plurality of die assemblies, the
3 wafer stack having a first wafer and a second wafer, a first die assembly of the
4 plurality of die assemblies being formed of at least a portion of the first wafer
5 and at least a portion of the second wafer;
6 exposing a portion of the first wafer by removing a portion of the
7 second wafer; and
8 dicing the exposed portion of the first wafer such that the first die
9 assembly is at least partially separated from the wafer stack.
- 1 2. The method of claim 1, wherein the first wafer and the second
2 wafer are arranged in an overlying relationship with each other and bonded
3 together to form the wafer stack.
- 1 3. The method of claim 1, wherein the first wafer includes a first
2 component, the first component being arranged adjacent to the second wafer,
3 the first component being configured to electrically communicate with a
4 component external to the wafer stack.
- 1 4. The method of claim 1, wherein the wafer stack includes a third
2 wafer, the second wafer being arranged at least partially between the first wafer
3 and the third wafer; and
4 wherein the step of exposing a portion of the first wafer comprises the
5 step of:
6 exposing a portion of the first wafer by removing a portion of the third
7 wafer and a portion of the second wafer.

1 5. The method of claim 1, wherein the step of exposing a portion of
2 the first wafer comprises the steps of:

3 dicing the second wafer to enable detachment of a portion of the second
4 wafer from the wafer stack; and

5 removing the portion of the second wafer from the wafer stack.

1 6. The method of claim 1, wherein the step of dicing the exposed
2 portion of the first wafer comprises the step of:

3 performing a through-cut of the wafer stack to at least partially detach
4 the first die assembly from the wafer stack.

1 7. The method of claim 3, wherein the second wafer defines a
2 recessed portion, the recessed portion being arranged in an overlying relationship
3 with the first component, the recessed portion being configured to enable a
4 partial through-cut of the second wafer in a vicinity of the recessed portion such
5 that the first component is not damaged during formation of the partial through-
6 cut; and

7 wherein the step of exposing a portion of the first wafer comprises the
8 step of:

9 performing a partial through-cut of the second wafer in the vicinity of the
10 recessed portion such that the first component is not damaged by the partial
11 through-cut.

1 8. The method of claim 4, wherein the step of exposing a portion of
2 the first wafer comprises the steps of:

3 exposing a portion of the second wafer by removing a portion of
4 the third wafer; and

5 exposing a portion of the first wafer by removing a portion of the
6 second wafer.

1 9. The method of claim 5, wherein the step of dicing the second
2 wafer comprises the step of:

3 performing a first partial through-cut and a second partial through-cut of
4 the wafer stack to at least partially detach of a portion of the second wafer from
5 the wafer stack, the portion of the second wafer to be detached being arranged
6 between the first partial through-cut and the second partial through-cut.

1 10. A die assembly formed by the method of claim 1.

1 11. A wafer stack defining a plurality of die assemblies, said wafer
2 stack comprising:

3 a first wafer including a first component; and

4 a second wafer arranged in an overlying relationship with said first wafer,
5 said second wafer being bonded to said first wafer, said first component being
6 arranged adjacent to said second wafer, said second wafer defining a recessed
7 portion, said recessed portion being arranged in an overlying relationship with
8 said first component, said recessed portion being configured to enable a partial
9 through-cut of said second wafer in a vicinity of said recessed portion such that
10 said first component is not damaged during formation of the partial through-cut;

11 wherein a first die assembly of the plurality of die assemblies is defined
12 by at least a portion of said first wafer and at least a portion of said second
13 wafer.

1 12. The wafer stack of claim 11, further comprising:

2 a third wafer, said second wafer being arranged at least partially between
3 said first wafer and said third wafer.

1 13. The wafer stack of claim 11, wherein said first component is
2 configured to enable communication of said first die assembly with a component
3 external to said first die assembly.

1 14. The wafer stack of claim 12, wherein said second wafer includes a
2 second component, and wherein said third wafer defines a recessed portion,
3 said recessed portion of said third wafer being arranged in an overlying
4 relationship with said second component, said recessed portion of said third
5 wafer being configured to enable a partial through-cut of said third wafer in a
6 vicinity of said recessed portion of said third wafer such that said second
7 component is not damaged during formation of the partial through-cut of said
8 third wafer.

1 15. The wafer stack of claim 12, wherein said second wafer has a
2 second component, and wherein said third wafer comprises means for enabling
3 a partial through-cut of said third wafer.

1 16. The wafer stack of claim 13, wherein said first component is
2 configured to enable electrical communication of said first die assembly with a
3 component external to said first die assembly.

1 17. The wafer stack of claim 15, wherein said means for enabling a
2 partial through-cut comprises means for preventing damage of said second
3 component.

1 18. A wafer stack defining a plurality of die assemblies, said wafer
2 stack comprising:
3 a first wafer including a first component; and
4 a second wafer arranged in an overlying relationship with said first wafer,
5 said second wafer being bonded to said first wafer, said first component being
6 arranged adjacent to said second wafer;
7 said first wafer and said second wafer defining a gap therebetween, said
8 gap being arranged in an overlying relationship with said first component, said
9 gap being configured to enable a partial through-cut of said second wafer in a
10 vicinity of said gap such that said first component is not damaged during
11 formation of the partial through-cut;
12 wherein a first die assembly of the plurality of die assemblies is defined
13 by at least a portion of said first wafer and at least a portion of said second
14 wafer.

1 19. The wafer stack of claim 18, wherein said gap is at least partially
2 defined by a recessed portion of said second wafer.

1 20. The wafer stack of claim 18, further comprising:
2 a third wafer, said second wafer being arranged at least partially between
3 said first wafer and said third wafer; and
4 wherein said second wafer has a second component, said third wafer
5 defining a recessed portion arranged in an overlying relationship with said
6 second component, said recessed portion of said third wafer being configured to
7 enable a partial through-cut of said third wafer in a vicinity of said recessed
8 portion of said third wafer such that said second component is not damaged
9 during formation of the partial through-cut of said third wafer.

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